Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently amended) A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising:

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage,

wherein the first state comprises at least a portion of a memory address of the first memory block.

2. (Original) The memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second state when the first memory segment is not available for data storage.

3. (Currently amended) The memory management circuit of claim 1, wherein the ~~first state and~~ second state ~~are states~~is a state of a single logic bit.

4. (Currently amended) The memory management circuit of claim 1, wherein the ~~first~~ second state ~~includes~~ comprises information of an offset to a next available memory block or memory segment~~at least a portion of a memory address of the first memory block~~.

5. (Original) The memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory segment is not available for data storage.

6. (Currently amended) The memory management circuit of claim 2, ~~further comprising a third logic circuit having a state indicative~~ wherein the first state of the second logic circuit comprises at least a portion of a memory address of the first memory segment.

7. (Original) The memory management circuit of claim 2, further comprising a third logic circuit that converts the first state of the first logic circuit and the first state of the second logic circuit to the memory address of the first memory segment.

8. (Currently amended) The memory management circuit of claim 2, wherein the first and second states of the first logic circuit are states of a ~~single~~ plurality of logic bits, and the first and second states of the second logic circuit are states of a ~~single digital~~plurality of logic bits.

9. (Currently amended) The memory management circuit of claim 2, wherein ~~the first state of the first logic circuit is indicative of a memory address of the first memory block and~~ the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment.

10. (Currently amended) A memory management circuit for managing a memory having a ~~first and second~~plurality of memory blocks, each memory block having a ~~first and second~~plurality of memory segments, the memory management circuit comprising:

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage;

wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block; ~~and~~

~~a second logic circuit having a first state when any of the memory segments of the second memory block are available for data storage and a second state when none of the memory segments of the second memory block are available for data storage~~.

11. (Currently amended) The memory management circuit of claim 10, further comprising:

a ~~third~~ second logic circuit having a first state when ~~the~~ a first memory segment of the

first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage~~; and~~

~~a fourth logic circuit having a first state when the second memory segment of the first memory block is available for data storage and a second state when the second memory segment of the first memory block is not available for data storage~~.

12. (Currently amended) The memory management circuit of claim 11, wherein the first and second states of the second logic circuit are single-bit logic states ~~further comprising:~~

~~a fifth logic circuit having a first state when the first memory segment of the second memory block is available for data storage and a second state when the first memory segment of the second memory block is not available for data storage; and~~

~~a sixth logic circuit having a first state when the second memory segment of the second memory block is available for data storage and a second state when the second memory segment of the second memory block is not available for data storage~~.

13. (Currently amended) A memory management ~~system~~ circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising:

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage;

wherein the second state of the first logic circuit comprises information indicating an offset to available memory

~~a first bitmap having a sequence of bits, each bit of the first bitmap corresponding to a respective one of the plurality of memory blocks, each bit of the first bitmap having a first logic state if the bit's respective memory block has a memory segment that is available for data storage and a second logic state if the bit's respective memory block does not have a memory segment that is available for data storage; and~~

~~a second bitmap having a sequence of bits, each bit of the second bitmap corresponding~~

~~to a respective one of the plurality of memory segments of the memory, each bit of the second bitmap having a first logic state if the bit's respective memory segment is available for data storage and a second logic state if the bit's respective memory segment is not available for data storage~~.

14. (Currently amended) The memory management ~~system~~ circuit of claim 13, further comprising a second logic circuit ~~that identifies a bit in the first bitmap having the first logic state~~having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for storage.

15. (Currently amended) The memory management system of claim ~~13~~14, wherein the second state of the second logic circuit comprises information indicating an offset to an available memory segment~~ further comprising a logic circuit that identifies a memory block having a memory segment available for data storage by identifying a first bit in the first bitmap having a state indicative of the first bit's respective memory block having a memory segment available for data storage, and identifies a memory segment that is available for data storage by identifying a second bit in the second bitmap having a logic state indicative of the second bit's respective memory segment being available for data storage~~.

16-23. (Canceled)

24. (Currently amended) A method for managing memory, the method comprising:

analyzing a state of a first logic circuit ~~first flag~~ to determine whether a block of memory segments includes a memory segment that is available for data storage, the first logic circuit having a first state when the block of memory segments has a memory segment that is available for data storage and a second state when the block of memory segments does not have a memory segment that is available for data storage; and

if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage.

25. (Currently amended) The method of claim 24, wherein the first state comprises at least a portion of a memory address of the block of memory segments ~~identifying a memory segment in the block of memory segments that is available for data storage comprises analyzing a second flag to determine whether a particular memory segment in the block of memory segments is available for data storage~~.

26. (Currently amended) The method of claim 24, wherein the first state comprises information indicating a number of available memory segments in the block of memory segments ~~identifying a memory segment in the block of memory segments that is available for data storage comprises:~~

~~analyzing a second flag to determine whether a first memory segment in the block of memory segments is available for data storage;~~

~~if the first memory segment in the block of memory segments is available for data storage, determining the address of the first memory segment; and~~

~~if the first memory segment in the block of memory segments is not available for data storage, analyzing a third flag to determine whether a second memory segment in the block of memory segments is available for data storage~~.

27. (Currently amended) The method of claim 26, wherein the second state comprises information indicating an offset to available memory ~~the first flag is a flag in an array of flags, and determining the address of the first memory segment comprises converting a position of the first flag in the array of flags to a most significant portion of the address of the first memory segment~~.

28-40. (Canceled)